A Modelling and Design Approach for Push/Pull Switched Capacitor DC-DC Converters

Athanasios Sarafianos
ESAT-MICAS
KU Leuven Kasteelpark Arenberg 10
B-3001 Leuven, Belgium
Email: asarafia@esat.kuleuven.be

Michiel Steyaert
ESAT-MICAS
KU Leuven Kasteelpark Arenberg 10
B-3001 Leuven, Belgium
Email: steyaert@esat.kuleuven.be

***Abstract*—This paper presents an extension to the switched capacitor DC-DC converter model when supplying loads stacked vertically. Stacking loads vertically drastically reduces the required size of a DC-DC converter, as it only needs to supply the mismatch current between the loads. Furthermore, when loads are perfectly matched, efficiency is only limited by the power consumption of the control loop, achieving efficiencies close to 100%. The proposed adapted model is extensively discussed, along with system level considerations regarding the required control loop. As a proof of concept, simulations of a transistor-level DC-DC converter that supplies three vertically stacked loads are shown.**

(Keywords: modelling, design, Push/Pull, Switched Capacitor, DC-DC Converter)

I. Introduction

Switched capacitor (SC) DC-DC converters show great promise to provide on-chip per-core down-conversion for digital loads, as several works showcase high power density [1], high voltage conversion ratio [2] and fast response time [3]. Unfortunately, the achievable efficiency and power density will ultimately be limited by the output impedance of the DC-DC converter, which translate to to I^2R-losses.

In the case of Fig. 1, the on-chip DC-DC converter needs to supply the full load current of 2.1A, leading to a large converter area. However, if these circuits can be stacked vertically, as in Fig. 2, an interesting opportunity arises. The on-chip DC-DC converter will no longer need to deliver the full output power, but only sink or source the difference in current consumed by the stacked loads, allowing a reduced converter area. When stacked loads consume equal amounts of power, implicit DC-DC down-conversion is achieved (similar to a resistive ladder), potentially achieving 100% efficiency at maximum load, while the DC-DC converter can essentially be idle. When loads are not identical, the converter shuttles charge from or to the loads, maintaining the output voltage at the desired level. At the load side, microprocessor cores or subblocks can still communicate with one another through the use of level shifters, as has been proposed and implemented in [4], [5].

Another benefit from stacking loads vertically is the reduction in supplied current by the bus voltage regulator. As more loads are stacked vertically, V_{BUS} can be increased while the input current decreases by the same factor, alleviating

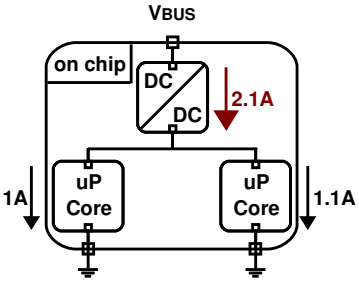


Fig. 1: A typical system with off-chip bus voltage regulation and an on-chip step-down converter.

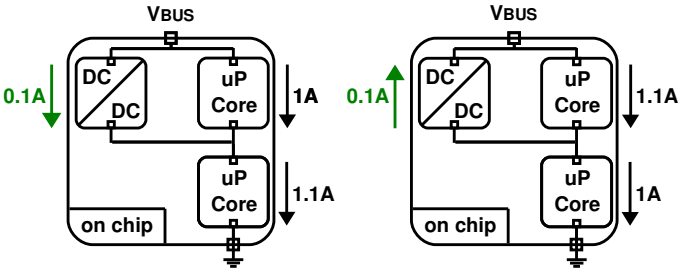


Fig. 2: Proposed system for stacked loads, with reduced current demands.

problems that may arise from voltage drops in the on-chip power distribution network [1]. While the power requirements for the bus converter remains the same, the reduced maximum current leads to reduced conduction losses, and can hence improve efficiency of the bus regulator. Furthermore, for a PWM-controlled buck converter, the higher output voltage leads to an increased duty cycle, leading to relaxed specifications for e.g. the levelshifters [6].

Non-SC solution exist, where linear regulators [4] or inductive converters [7] are used to supply these stacked loads. The latter are not very well suited for full integration, as inductors are not easily integrated without additional (costly) processing steps, and the design of [7] makes use of coupled inductors. Push/pull linear regulators as in [4] show great promise, but the high biasing currents required for the regulators still limit the efficiency at around 80-90%, even at matched loads.

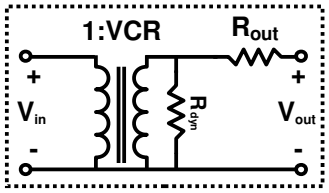


Fig. 3: Switched capacitor model, from [10].

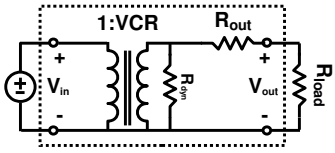


Fig. 4: Single load example.

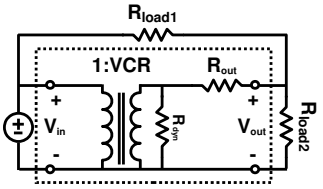


Fig. 5: Stacked loads example.

SC converters that try to tackle the problem of push/pull SC converters do this with only moderate success [8], [9]: a steady-state output voltage droop occurs for increasing mismatch currents, while providing little insight into their design. In [5], a symmetrical ladder SC converter is used to supply 4x4 stacked microprocessor cores, but is grossly oversized for the amount of mismatch current it needs to supply, in an effort to minimize this droop. In this paper, we will show that we can get rid of this droop by implementing not one, but two SC-topologies per converter, yielding a compacter solution.

In Section II, the switched capacitor model proposed by [10] will be examined, and the requirements of a DC-DC converter to truly operate in a push/pull manner will be deduced. Section III will discuss control loops for push/pull SC converters, while Section IV will show the simulation results of a transistor-level implementation of such a DC-DC converter with control loop, before drawing conclusions in Section V.

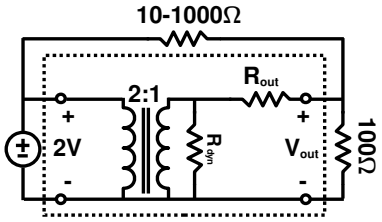
II. Switched Capacitor Model

Fig. 3 shows the SC model proposed by [10]. The output impedance is given by $R_{out} = \sqrt{R_{fsl}^2 + R_{ssl}^2}$, with R_{fsl} the fast switching limit (FSL) impedance, determined by the resistance of the switches, and R_{ssl} the slow switching limit (SSL) impedance, modelling the losses associated with charging and discharging the flying capacitors non-adiabatically. The extra parallel impedance R_{dyn} can be added to model the losses associated with parasitic bottom plate losses, switch gate drive losses and losses associated with the ESR of the capacitors.

Consider the circuit in Fig .4, where a single converter supplies a load R_{load}. In this case, V_{out} is given by:

$$V_{out} = V_{in} VCR \frac{R_{load}}{R_{load} + R_{out}} \tag{1}$$

For given load requirements and input voltage, designers have



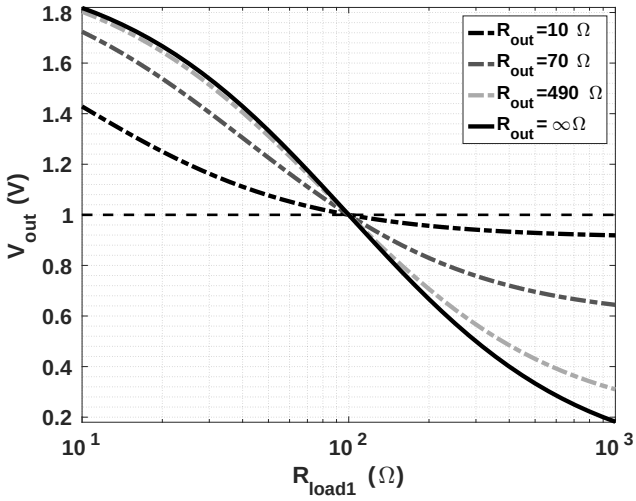


Fig. 6: Numerical example and output voltage in function of R_{load1}.

the freedom of choosing the voltage conversion ratio (VCR) of the SC converter, and it's output impedance (size of switches, capacitors and switching frequency). When loads operate over a wide output voltage, multiple VCRs are combined in a gearbox converter to cover this larger range efficiently [1], [3]. This equation is no longer valid for modelling stacked loads, as in Fig. 5. The output voltage does not only depend on the value of R_{load1}, but also on R_{load2}.

$$V_{out} = \frac{V_{in}(R_{load1} VCR - R_{out}) R_{load2}}{(R_{load1} R_{load2} - R_{load1} R_{out} - R_{load2} R_{out})} \tag{2}$$

While this equation is the result of simply applying Kirchhoff's laws, it offers little insight. To help clarify the meaning of this equation, Fig. 6 shows a numerical example. Imagine the loads require an output voltage of $1V$, $R_{load_2} = 100\Omega$, $R_{load1} = 10\Omega - 1k\Omega$, and the converter uses $VCR = 1/2$ (i.e. the ideal step-down ratio). As long as $R_{load1} > R_{load2}$, V_{out} remains close to 1V, but does not achieve the desired 1V operating point. If $R_{load1} < R_{load2}$, the output voltage rapidly diverges from $1V$. Only when $R_{load1} = R_{load2}$ is the output voltage exactly $1V$, although in this specific case, no converter is required, as the loads perform implicit down-conversion. The culprit for this behaviour is the output impedance R_{out}. While the ideal (i.e. unloaded) output voltage is indeed $1V$, any current delivered by the converter will induce a voltage drop over R_{out}, which will be forward when $R_{load1} > R_{load2}$, and reverse when $R_{load1} < R_{load2}$. Graphically, the same conclusion can be drawn, since every curve intersects the

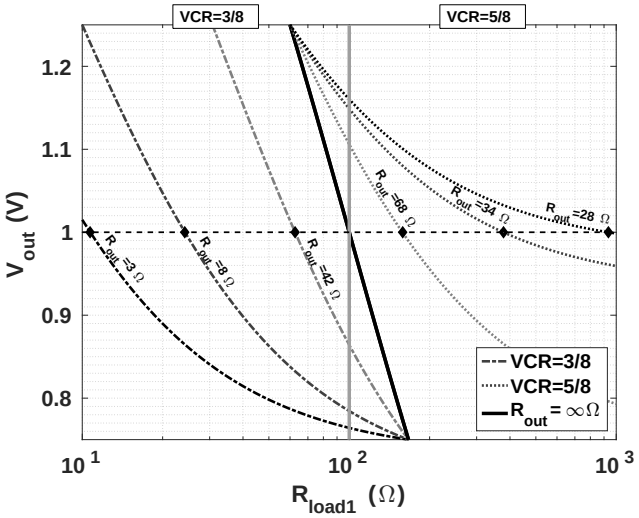


Fig. 7: V_{out} in function of R_{load1}, using two discrete VCRs. Each line intersects the $1V$-horizontal at different values of R_{load1}.

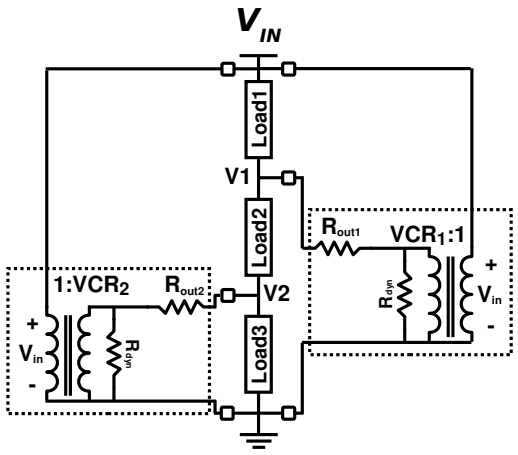


Fig. 8: Model of a system with three vertically stacked loads and two converters, regulating the intermediate nodes.

$1V$-horizontal at the point where $R_{load1} = R_{load2}$. All valid operating points are constrained by two limits: the $1V$-horizontal, representing $R_{out} = 0\Omega$, and the curve where $R_{out} = \infty\Omega$.

However, there is a way to cope with this. In [5], [8], [9], only 1 VCR is implemented, where R_{out} is made as small as possible to reduce the voltage drop, coming at a hefty price of area overhead. Instead, we propose to use at least 2 discrete VCRs:

1) $VCR > V_{out,desired}/V_{in}$, able to regulate the output as long as $R_{load1} > R_{load2}$ ($I_{load1} < I_{load2}$). This VCR will source (push) current to the output.
2) $VCR < V_{out,desired}/V_{in}$, able to regulate the output as long as $R_{load1} < R_{load2}$ ($I_{load1} > I_{load2}$). This VCR will sink (pull) current from the output.

Using eq. 2, but now selecting two VCRs according to the above criteria (e.g. VCR=3/8 and VCR=5/8), shows that for each value of R_{load1}, an according output impedance can be calulated to regulate the output to 1V. To visually support this, Fig. 7 shows the output voltage in function of R_{load1} for varying R_{out}. Each intersection with the $1V$-horizontal represents a valid operating point.

The equations that were earlier derived can be further simplified, if the loads are modelled as current sources with a minimum and maximum current consumption. In this case, V_{out} can be calculated using the following formula:

$$V_{out,i} = V_{in} VCR_i + (I_{Load,i} - I_{Load,i+1}) R_{out,i} \quad (3)$$

leading to a more insightful equation, with index i denoting the regulated node, as in Fig. 11. Another formula that is used during the design of SC converters, gives the output ripple when operating in the SSL-region:

$$\Delta V_{out,i} = \frac{I_{out,i}}{2N_{frag}(C_o + \kappa_\tau C_{fly,tot,i}) f_{sw,i}} \quad (4)$$

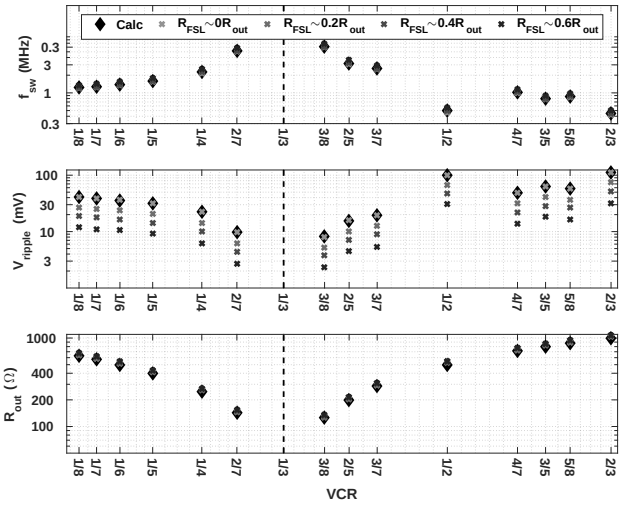


Fig. 9: Calculated vs. simulated values for f_{sw}, V_{ripple} and R_{out} in function of VCR.

with $I_{out,i}$ the current delivered by the converter, N_{frag} the amount of out-of-phase fragments [11], C_o the output capacitance, κ_τ a topology-defined constant, $C_{fly,tot,i}$ the total amount of flying capacitance used in converter i, and $f_{sw,i}$ the switching frequency of converter i. This equation by expressing the output current of the converter as:

$$\Delta I_{out,i} = \frac{V_{in} VCR_i - V_{out,i}}{R_{out,i}} \quad (5)$$

and assuming that the contribution of R_{SSL} in R_{out} dominates:

$$R_{out,i} = \frac{K_C}{f_{sw,i} C_{fly,tot,i}} \quad (6)$$

Filling in these two formulas in 4 leads to the following result:

$$\Delta V_i = \frac{C_{fly,tot,i}(V_{in}VCR_i - V_{out,i})}{K_C 2N_{frag}(C_o + \kappa_\tau C_{fly,tot,i})} \quad (7)$$

with K_C a topological constant [11]. This result leads to some interesting conclusions. When operating in the SSL-region, the amount of ripple can be set by choosing the VCR, along with the obvious amount of fragmentation and on-chip capacitance. To further support this conclusion, assume three loads stacked vertically, as in Fig. 8. Assume an input voltage of 3V, while the internal nodes are regulated to 2V and 1V. For node $V_2 = 1V$, several VCRs are compared to one another regarding required switching frequency, output ripple and output impedance, for a given area ($C_{fly,tot} = 1nF$, $C_o = 10nF$) and maximum output current ($I_{out} = \pm 1mA$). For each VCR, the above formulas are used and then compared to simulation results, for varying values of R_{fsl} ($R_{fsl} \cong 0/0.2/0.4/0.6R_{out}$).

Fig. 9 compares the simulated values with the calculated values. The calculated results match very closely to the simulated values, where $R_{fsl} \sim 0$. For larger values of R_{fsl}, f_{sw} and R_{out} still remain reasonably close to the predicted values, although strictly speaking the converters no longer operate in the SSL-region (eq. 4). The ripple however does show some significant deviation for increasing R_{fsl}. When moving towards the FSL-region, the dampening effect of the on-resistance of the switches becomes non-negligible, leading to the lower output ripples. However, the calculated results can still be viewed as a theoretical upper bound on ripple, and are close approximations at reduced output powers [11], where R_{SSL} dominates.

III. Control Loop of a Push/Pull SC Converter

More and more SC converter designs use a digital hysteretic control loop to regulate their output voltage. The main advantages are very high bandwidth/fast response times, straightforward operation and robustness [2] [1]. In a simple single load SC converter, a hysteretic controller will toggle the state of the power converter ($\phi_1 \leftrightarrow \phi_2$) whenever the output voltage is lower than the reference voltage at the clocking instance. However, thanks to the symmetrical nature of the strong-arm comparator [1], a pulse will also be generated whenever the output is higher than the reference voltage. These dual outputs enable the control of push/pull converters: when pushing, use the output that toggles when $V_{out} < V_{ref}$ (outp), while the output that toggles when $V_{out} < V_{ref}$ should be used when pulling (outn) (Fig. 10).

To decide whether the converter should push or pull, a control loop is required that monitors the current consumption of the loads. One way to do so is to insert sensing resistors in series with the loads, and use the voltage drops over these resistors to decide whether the converter should be pulling or pushing. However, direct access to the current paths of the loads might not be available, and a trade-off exists between power lost by these sensing resistors and amplitude of the sensing voltage. Bigger resistors lead to a larger sensing voltage, but also larger I^2R-losses. Small sensing resistors reduce these losses, but the resulting small signals require high precision comparators (which in turn consume a large amount of power) to correctly decide the mode.

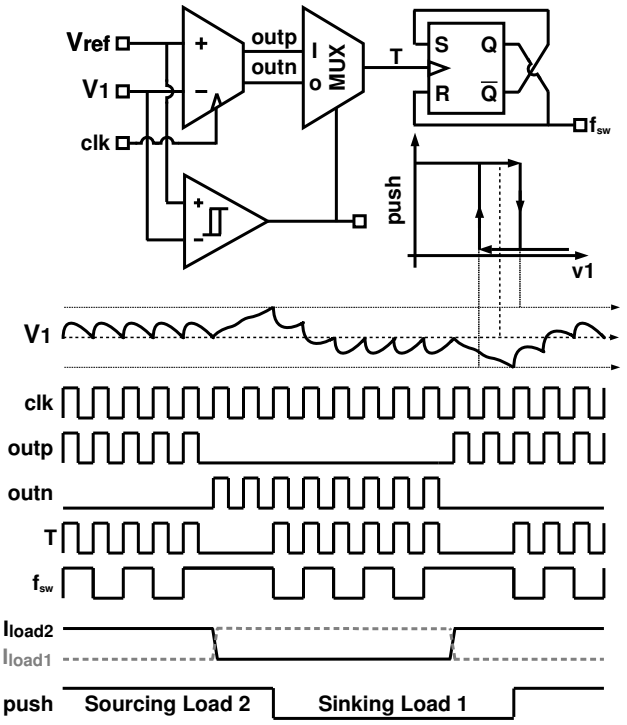


Fig. 10: Operation of the adapted hysteretic voltage control, along with the push/pull comparator.

Another way to do so is to monitor the output voltage by means of a single comparator with hysteresis. As long as the monitored node remains within the hysteresis band, no change in mode occurs. Whenever the output voltage exceeds the hysteresis band, the converter should switch modes. Fig. 10 shows the proposed control loop. At first, I_{load2} is larger than I_{load1}, and the hysteretic controller toggles each time the output voltage drops below the reference voltage (while $push = 1$). When I_{load2} enters a low-activity state and I_{load1} draws more current, the output voltage rises at first ($V_1 > V_{ref}$, converters remains inactive). Once the output voltage crosses the threshold of the comparator with hysteresis, a mode change occurs ($push = 0$), and the converter starts pulling down the output voltage again, regulating the output voltage once more, pulling current from Load1. The same behaviour occurs when Load2 again starts drawing more current than Load1. While using only conventional circuits, the combination yields a new type of control loop for push/pull SC converters.

IV. Simulations of an Example Converter

To validate the model and the conclusions previously drawn, a complete transistor-level design has been made and simulated, using a 65nm CMOS design kit. Fig. 11 shows an overview of the implemented system. Three loads are stacked

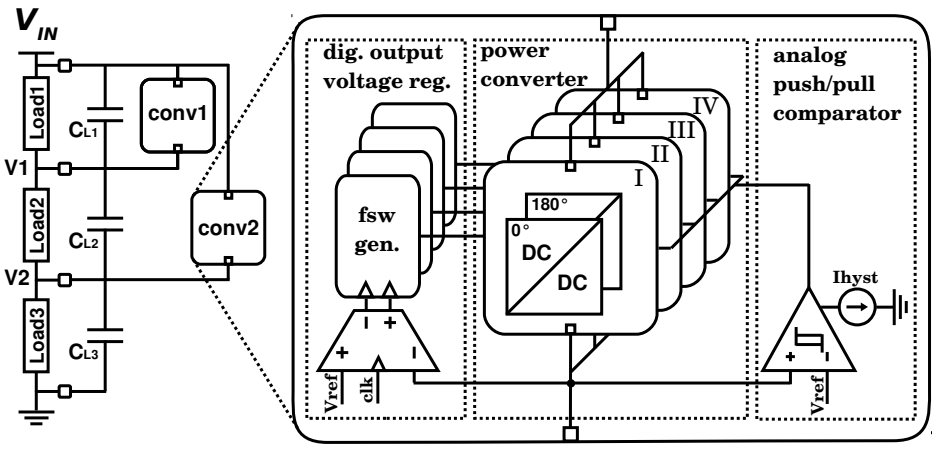


Fig. 11: Three loads stacked vertically and two converters, with the block level visualisation of one of the converters. Each converter has an identical control loop, but a different topological implementation.

vertically up to the input voltage of 3V, and each internal node is supplied by its own push/pull SC converter. These converters are each regulated by a separate control loop, consisting of a digital hysteretic control loop, and an analog comparator with hysteresis, as in Fig. 10. Each converter has its input connected to the input voltage, leading to a different topological implementation of the power converters (Fig.11). For output node V_1, the power converter is implemented using topologies $VCR_{push} = 5/7$ and $VCR_{pull} = 3/5$, while the converter supplying node V_2 uses topologies $VCR_{push} = 2/5$ and $VCR_{pull} = 2/7$. The transistor-level implementation and their capacitor arrangement in each phase is shown in Fig. 12.

Each power converter consists of an in-phase (0°) and an anti-phase (180°) part, leading to symmetrical charge transfer to the load in both phases. The power converter is then implemented using four such fragments, operated out-of-phase, to reduce output ripple [11]. The control loops however, are identical for both converters, and operate at identical clock frequencies, yet shifted by 180° with regards to each other. The control loop operation is identical to the control loop as explained in Section III.

The designed system has been extensively simulated, for load steps of $20mA \leftrightarrow 80mA$ ($50\Omega \leftrightarrow 12.5\Omega$), so that each converter needs to supply $\pm 60mA$, while load steps occur with rise/fall times of 100ps. Fig. 13 shows the output voltages, load currents and the push/pull decisions of the control loop. The converter maintains regulation for every operating point, while non-zero transient droops are only visible when switching from push to pull mode, or vice versa (as in Fig. 10). Fig. 14 shows the load voltages, load currents, and the achieved efficiencies for each of these operating points. This plot highlights the main advantage of stacking loads vertically: the high achievable efficiency when loads are closely matched. In this case where loads consume equal power, efficiencies of $> 98\%$ can be achieved, limited only by the power consumption of the control loop. Even when large mismatch currents are flowing

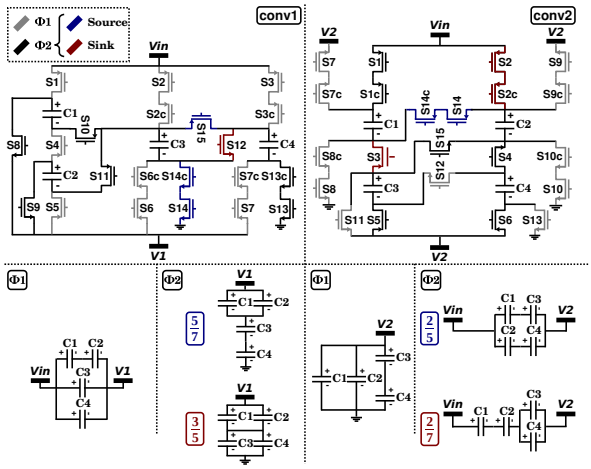


Fig. 12: Transistor-level implementation of the different conversion ratios.

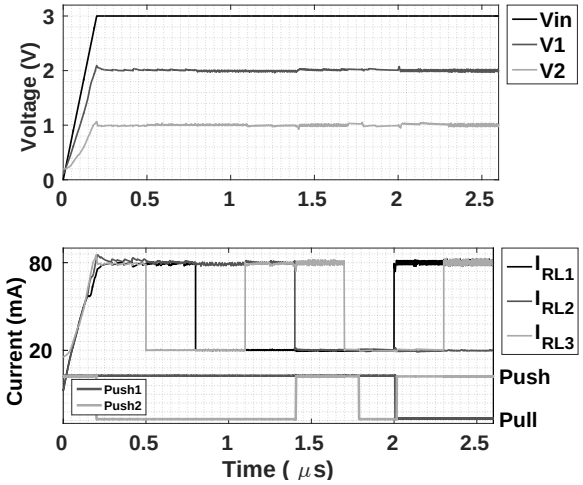


Fig. 13: Output voltage, Push/pull decision and load step simulation.

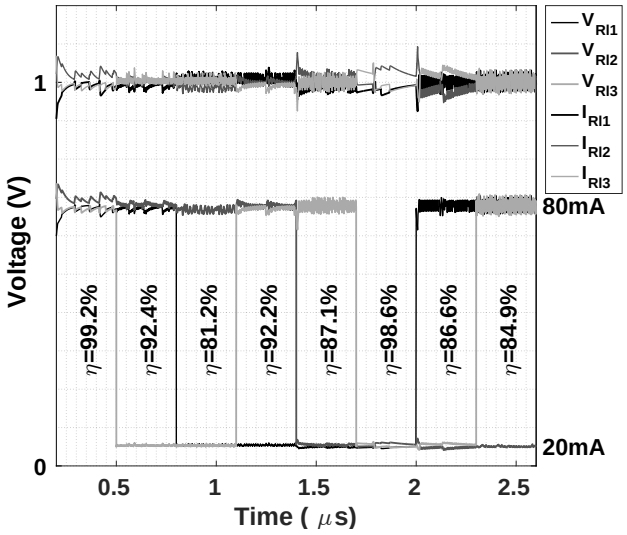


Fig. 14: Load voltages and achieved efficiencies.

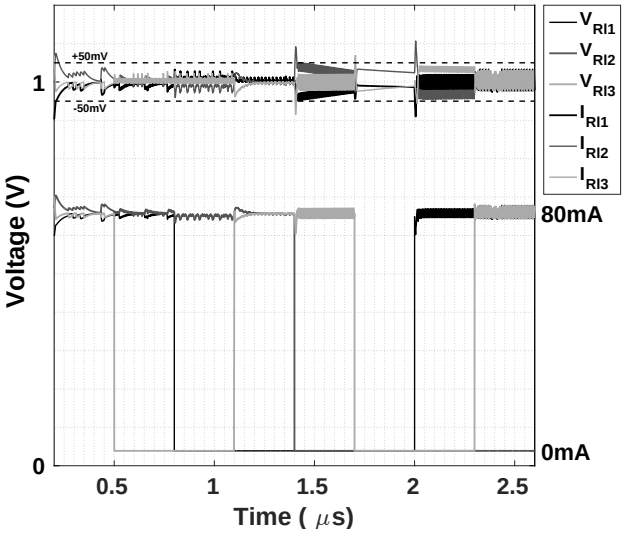


Fig. 15: Load voltages when loads drop to 0mA.

($I_{Rl1} = I_{Rl3} = 20mA$, $I_{Rl2} = 80mA$), a high efficiency of 81% is attained.

This converter has been designed to supply a mismatch current of up to 60mA. While in our situation we assumed a minimal power consumption of 20mW by the loads, the converter is also able to cope with loads that turn off completely ($\sim 0mW$ power consumption). In this situation, the maximum power consumption of the loads should be restricted to 60mW. However, Fig. 15 shows the load voltages when loads, with a maximum power consumption of 80mW, suddenly drop away. As can be seen, the load voltages remain within ±50mV of the intended output voltage. While unforseen, these load voltages would not cause overvoltage stress, and hence guarantee safe operation of the loads.

V. Conclusion

In this paper, the validity of extending Seeman's model [10] of SC DC-DC converters for supplying vertically stacked loads has been discussed. It has been shown that for each output voltage, two VCRs need to be chosen, one that is higher than the ideal step down ratio, and one that is lower. From this, formulas were deduced that can be used as a first design guideline for designing such push/pull SC converters. These calculations have been compared to simulation results, and are shown to be in good accordance. Furthermore, implications for the required control loop have been discussed, and a block level implementation has been proposed. Finally, a full transistor-level design has been simulated, of which the results validate the operation of the system, and highlight the superior achieved efficiencies.

References

[1] T. Andersen, F. Krismer, J. Kolar, T. Toifl, C. Menolfi, L. Kull, T. Morf, M. Kossel, M. Braendli, and P. Francese, "A 10 w on-chip switched capacitor voltage regulator with feedforward regulation capability for granular microprocessor power delivery," *Power Electronics, IEEE Transactions on*, 2016.

[2] H. Meyvaert, G. Villar Pique, R. Karadi, H. Bergveld, and M. Steyaert, "A light-load-efficient 11/1 switched-capacitor dc-dc converter with 94.7efficiency while delivering 100 mw at 3.3 v," *Solid-State Circuits, IEEE Journal of*, vol. 50, no. 12, pp. 2849–2860, Dec 2015.

[3] H.-P. Le, J. Crossley, S. Sanders, and E. Alon, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19w/mm2 at 73% efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb 2013, pp. 372–373.

[4] S. Rajapandian, K. L. Shepard, P. Hazucha, and T. Karnik, "High-voltage power delivery through charge recycling," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1400–1410, June 2006.

[5] S. K. Lee, T. Tong, X. Zhang, D. Brooks, and G. Y. Wei, "A 16-core voltage-stacked system with an integrated switched-capacitor dc-dc converter," in *2015 Symposium on VLSI Circuits (VLSI Circuits)*, June 2015, pp. 318–319.

[6] J. Wittmann, T. Rosahl, and B. Wicht, "A 50v high-speed level shifter with high dv/dt immunity for multi-mhz dcdc converters," in *European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014 - 40th*, Sept 2014, pp. 151–154.

[7] K. Kesarwani, C. Schaef, C. R. Sullivan, and J. T. Stauth, "A multi-level ladder converter supporting vertically-stacked digital voltage domains," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, March 2013, pp. 429–434.

[8] L. Chang, R. Montoye, B. Ji, A. Weger, K. Stawiasz, and R. Dennard, "A fully-integrated switched-capacitor 2:1 voltage converter with regulation capability and 90% efficiency at 2.3a/mm2," in *Proc. on VLSI Circuits*, June 2010, pp. 55–56.

[9] K. Mazumdar and M. Stan, "Charge recycling on-chip dc-dc conversion for near-threshold operation," in *Subthreshold Microelectronics Conference (SubVT), 2012 IEEE*, Oct 2012, pp. 1–3.

[10] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," in *Computers in Power Electronics, 2006. COMPEL '06. IEEE Workshops on*, July 2006, pp. 216–224.

[11] T. Van Breussegem and M. Steyaert, "Monolithic capacitive dc-dc converter with single boundary multiphase control and voltage domain stacking in 90 nm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 7, pp. 1715–1727, July 2011.